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A Harmonic Circulation Current Reduction Method for Parallel Operation of UPS with a Three-Phase PWM Inverter

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ABSTRACT

In a parallel operation of UPS, there are two types of circulating currents between UPS. One is the low order circulating current with a fundamental frequency caused by the amplitude and phase differences of UPS output voltages, and the other is the harmonic circulating current with PWM switching frequency caused by non-synchronized PWM waveforms among UPS. The elimination of the low order circulating current is essential for optimal load sharing in parallel operations of UPS, which can be accomplished by the phase and magnitude control at each UPS. The harmonic circulating current may cause troubles and deteriorate in performance of the controller for optimal load sharing in parallel operation of UPS. This paper presents a PWM synchronizing method to eliminate the harmonic circulation current in parallel operation of UPS. The effectiveness of the proposed scheme has been investigated and verified through experiments by a 50kVA UPS.

Keywords: parallel operation UPS(Uninterruptible Power Supply), PWM synchronization, circulation current

1. Introduction

Parallel operation of UPS(Uninterruptible Power Supply) is needed to secure higher reliability through the redundant operation or in the step up of UPS capacity in the market. The heart of the parallel operation of UPS is the acceptable load sharing that each UPS have an equal split of the load. The good load sharing can be accomplished through the minimization of the circulation current flowing between UPSs. If it is assumed that the UPS inverter is an ideal sinusoidal voltage source, the circulation current is created only by the phase and magnitude difference of the output voltage between UPSs. Various kind of control schemes have proposed in order to reduce the circulation current under the assumption that UPS inverter is an ideal sinusoidal voltage source [1-4].

However, UPS inverter is not an ideal sinusoidal voltage source. Actually, the UPS inverter generates voltage of PWM(Pulse Width Modulation) waveform, which should be duly considered in parallel operation of UPS.

Generally, each UPS connected in parallel has an individual control board, each control board has a different timer interrupt signal for PWM generation, and likewise each UPS inverter will produce a different PWM voltage. As the result of the non-synchronized PWM voltage waveform between UPSs, a considerable amount of heightened harmonic circulation current with PWM

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switching frequency is created. This harmonic circulation current causes deterioration of the frequency control performance for a load sharing in proposed control schemes. Therefore, the elimination of not only the low order circulation current but also the harmonic circulation current is essential for the parallel operation of UPS. This paper proposes a simple PWM synchronizing method to eliminate the higher harmonic circulation current due to non-synchronizes PWM voltage using CAN (Controller Area Network) bus. In order to eliminate the low order circulation current, the method shown in[1] is used in this paper. The effectiveness of the proposed control scheme is verified by an experimental UPS system that has 50kVA load power capacity.

2. Proposed Control Structure

Fig. 1 shows parallel UPS system composed of two UPS. In this system, UPS_M is a master UPS and UPS_S is a slave UPS. Master and slave UPS share each other's information through CAN (Controller Area Network) bus. This communication line is essential for the parallel operation of UPS, some data communicated through the line are originally used for the elimination of the low order circulation current. Fig. 2 shows the data frame communicated through CAN bus. Its length consists of 76 bits. Arbitration field has the identification of the master or the slave, data field has the output current, bypass voltage, and some operation status. Each UPS transmits its own data frame to another UPS every 2ms. At that point, the master UPS has the highest priority. Each control board has two DSP (Digital Signal Processor) - one is a TMS320VC33 which is the main controller and the other is TMS320LF 2407A which generates the timer interrupt signal for PWM generation. Since each UPS calculates the total load current by summation of each UPS output current that is obtained trough CAN communication, the load current sensor for measuring the total load current is not necessary. A circulation current is calculated from the total load current divided by the number of parallel operating inverter. If one of two UPS fails to operation, the controller in the failed UPS detects the fault state and separates from the system by itself and the other UPS supplies the power to the load.

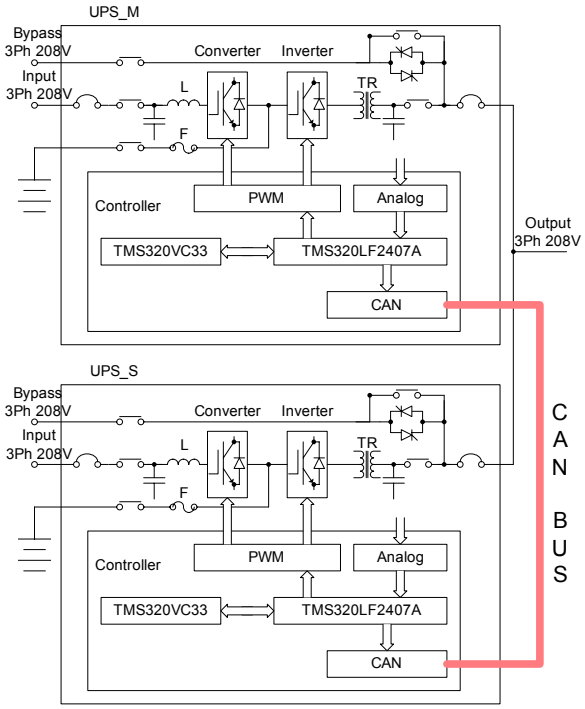


Fig. 1 Configuration of parallel UPS system

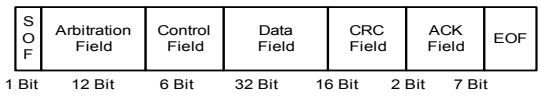


Fig. 2 Data frame of CAN bus

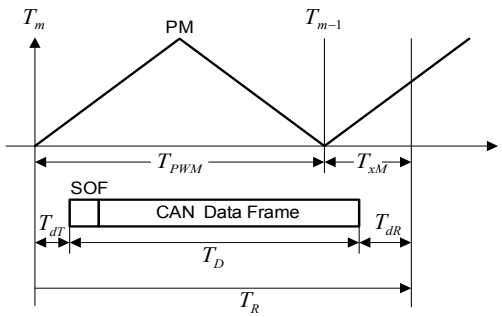


Fig. 3 Timer for PWM at Master UPS

3. PWM Synchronization

Figure 3 shows the relationship between the timers interrupt of matter UPS and the data frame shown in figure 2. In figure 3, PM is the period value of timer, T_{pwm} is period time, and T_m (m=0,1,2…) is the timer stating

point and T_{dT}, T_{dR} is the transmit interrupt latency and the received interrupt latency respectively. If it is assumed that master UPS transmits the data frame at T_m and slave UPS acknowledged the receive interrupt at $t = T_R$, the total time from the starting to the receive interrupt, T_R can be expressed as

$$T_R = T_{dT} + T_D + T_{dR} \quad (1)$$

Therefore the interval time between T_R and T_m, T_{xM} is

$$T_{xM} = T_{PWM} - T_R \quad (2)$$

where $|T_{xM}| < T_{PWM}/2$

Figure 4 shows the relationship between the timer interrupt of slave UPS and the data frame. In the figure, PS is the period of timer, T_s (s=0,1,2…) is the stating point of slave timer, UPWARD means the up-count interval, and DOWNWARD means the down-count interval. It is assumed that slave timer interrupt is generated at $t = t_{x(up)}$ during UPWARD mode, the time t_{xS} can be represented as

$$t_{xS} = t_x \quad (3)$$

where t_x is time corresponding to current value of slave timer. Then the difference time between T_m and T_s, t_{MS} can be expressed as

$$t_{MS} = T_m - T_s = t_{xS} + T_{xM} \quad (4)$$

Similarly, during downward mode

$$t_{xS} = T_{PWM} - t_x \quad (5)$$

$$t_{MS} = T_m - T_s = t_{xS} - T_{xM} \quad (6)$$

If the slave UPS calculates t_{MS} as (4), (6) whenever a receive timer is generated, slave is able to know if slave timer is leading or lagging behind the master timer. Figure 5 shows all cases which can be set up during upward mode. Figure 6 shows all cases during downward mode. Therefore, PWM synchronization can be accomplished as follow

- $PS \leftarrow T_{PWM} + \Delta T$ if slave timer is leading
- $PS \leftarrow T_{PWM} - \Delta T$ if slave timer lagging

This is to say, a slave timer value increases if it is ahead of the master timer. Conversely it decreases in case of lagging. Figure 7 shows the program flowchart for PWM synchronization.

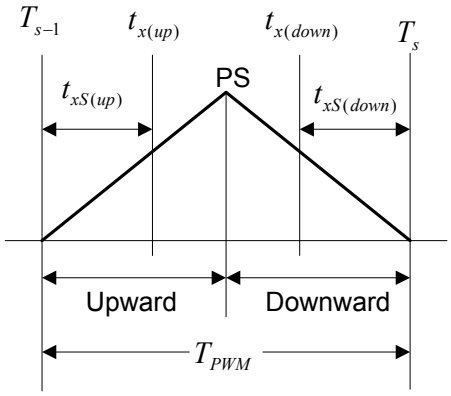


Fig. 4 Timer for PWM at Slave UPS

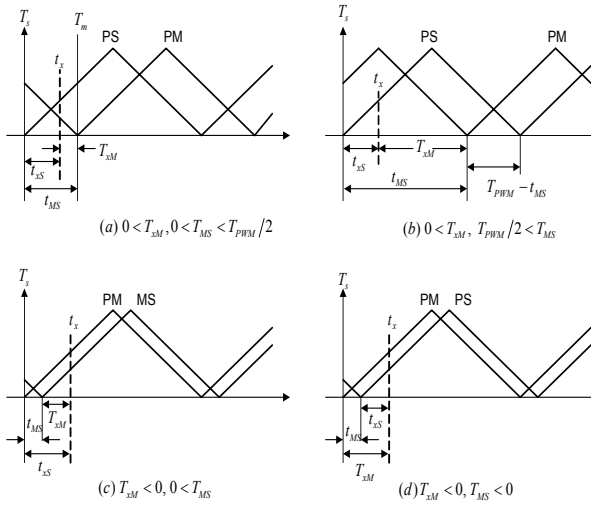
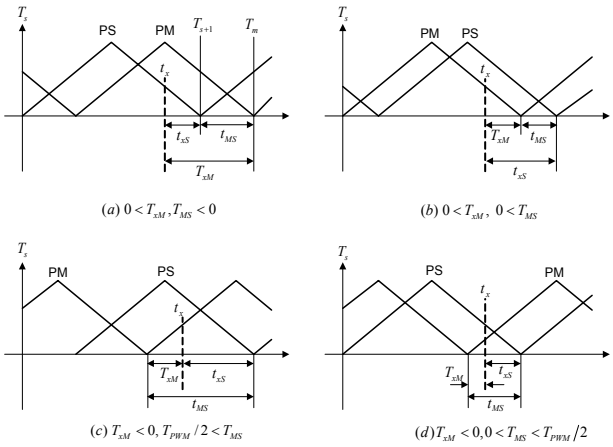


Fig. 5 All cases in Upward Mode

4. Experimental Results

The prototype of the fully digital controlled three-phase inverter using two DSP(TMS320C33 and TMS320LF2407A)



(a) $0 < T_{xM}, T_{MS} < 0$ (b) $0 < T_{xM}, 0 < T_{MS}$

(c) $T_{xM} < 0, T_{PWM}/2 < T_{MS}$ (d) $T_{xM} < 0, 0 < T_{MS} < T_{PWM}/2$

Fig. 6 All cases in Downward Mode

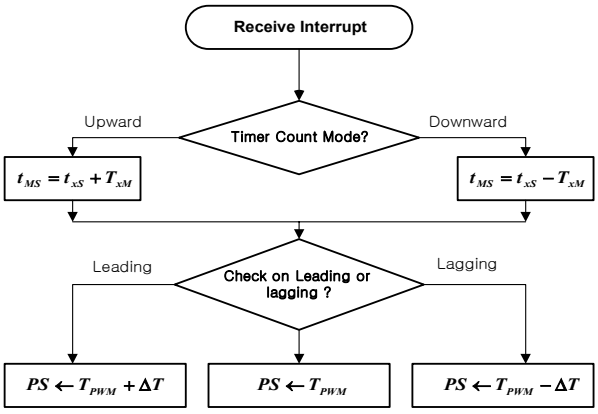


Fig. 7 Control Flow Chart

was built to investigate the operation performance and to prove the feasibility of the proposed method. The major parameters of the UPS system used in the experiments are given as follows

- Power rating : 50kVA
- Fundamental frequency : 60Hz
- Nominal line-to-line output voltage : 208V
- Inverter and converter switching frequency : 6kHz
- Output transformer turns ratio : 1.22:1
- Output transformer parameters:%X=5%, %R=3.5%
- Bus and Baud: CAN bus, 500Kbps

Under the no-load condition, figure 8-11 demonstrates the performance the parallel operation of UPS. Figure 8 show the output voltage and current waveform of matter UPS under the no-load state without any compensation for PWM synchronization. Note that the higher harmonic circulation current with PWM switching frequency is created by a non-synchronized PWM voltage wave between UPSs. Figure 9 shows PWM output voltage and the output current waveform of each UPS under the no-load condition. Figure 9(a) is for the case without compensation of PWM synchronization and (b) is the case of with compensation shown in proposed method in this paper. Note that the higher harmonic circulation current is considerably reduced. Figure 10 shows the output current waveform of each UPS connected in parallel under the rated load. Figure 10(a) is for the case without compensation and (b) is the case with compensation. Figure 10(b) shows that there is no harmonic circulation current and perfect load sharing, while figure 10(a) shows some harmonic circulation current and some phase difference in current of each UPS connected in parallel under the deteriorated load sharing. Figure 11 is the Fourier spectra of the output currents shown in figure10. Note that figure 11(a) shows that the current shown in figure 10(a) have a harmonic component of PWM switching frequency while there is no harmonic component in current waveforms shown in figure 10(b). These experimental results show that the harmonic circulation current can be eliminated by the proposed method in parallel operation of UPS.

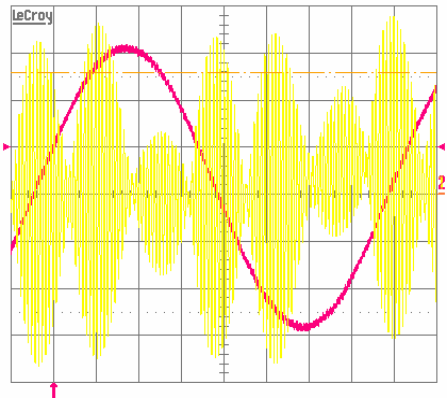
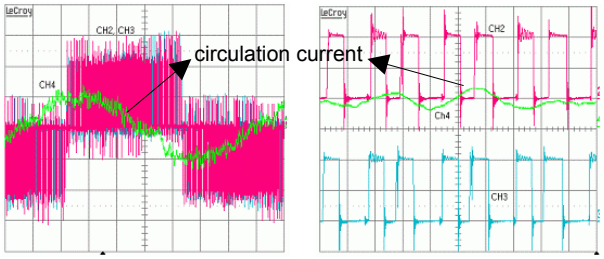
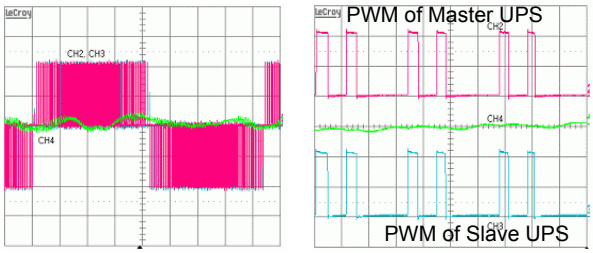


Fig. 8 Harmonic circulation current waveform flowing over output terminal of Master UPS under no-load state

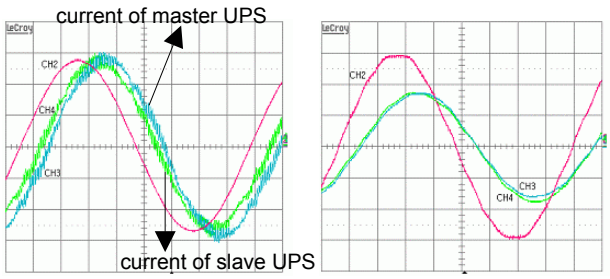


a) Without compensation



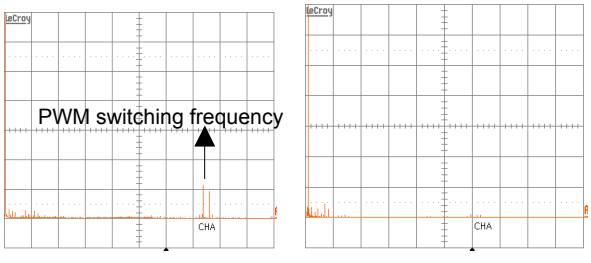
b) With compensation

Fig. 9 PWM output waveforms of each UPS and current waveform of master UPS under no-load state



a) Without compensation b) with compensation

Fig. 10 Current waveform of each UPS connected in parallel and UPS Output voltage waveform under rated load state



a) without compensation b)with compensation

Fig. 11 Fourier spectra of output current waveform of master UPS

5. Conclusions

This paper has proposed the PWM synchronizing method to eliminate the harmonic circulation current caused by non-synchronized PWM output voltage in parallel operation of UPS. This proposed method improves the performance of the frequency controller for the elimination of the circulation current with a fundamental frequency. Likewise it contributes to optimal load sharing in parallel UPS operation. The EMI problem also can be reduced by this proposed method. The proposed algorithm is very simple and it can be applied to the paralleled UPS operation having more than two UPS.

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